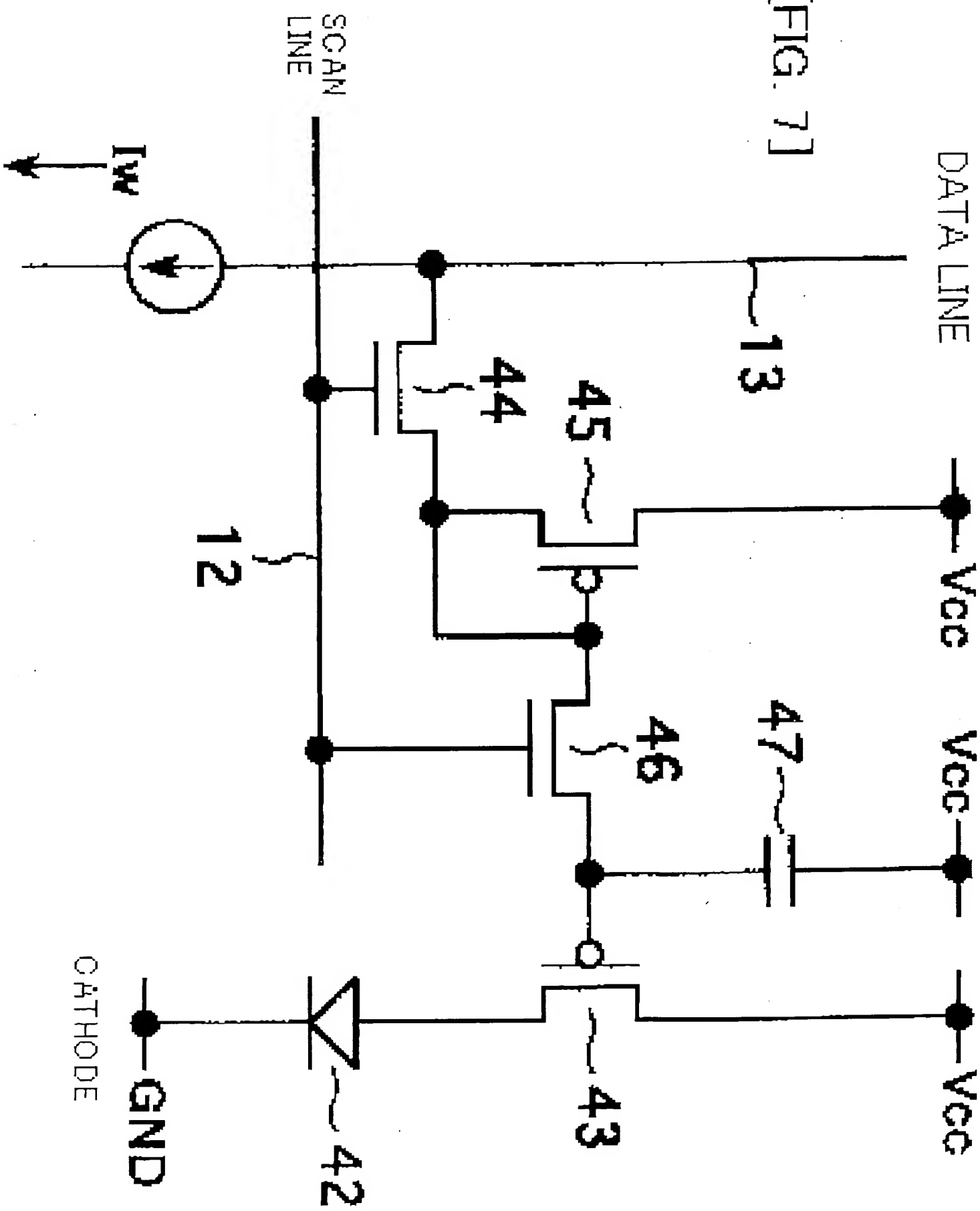
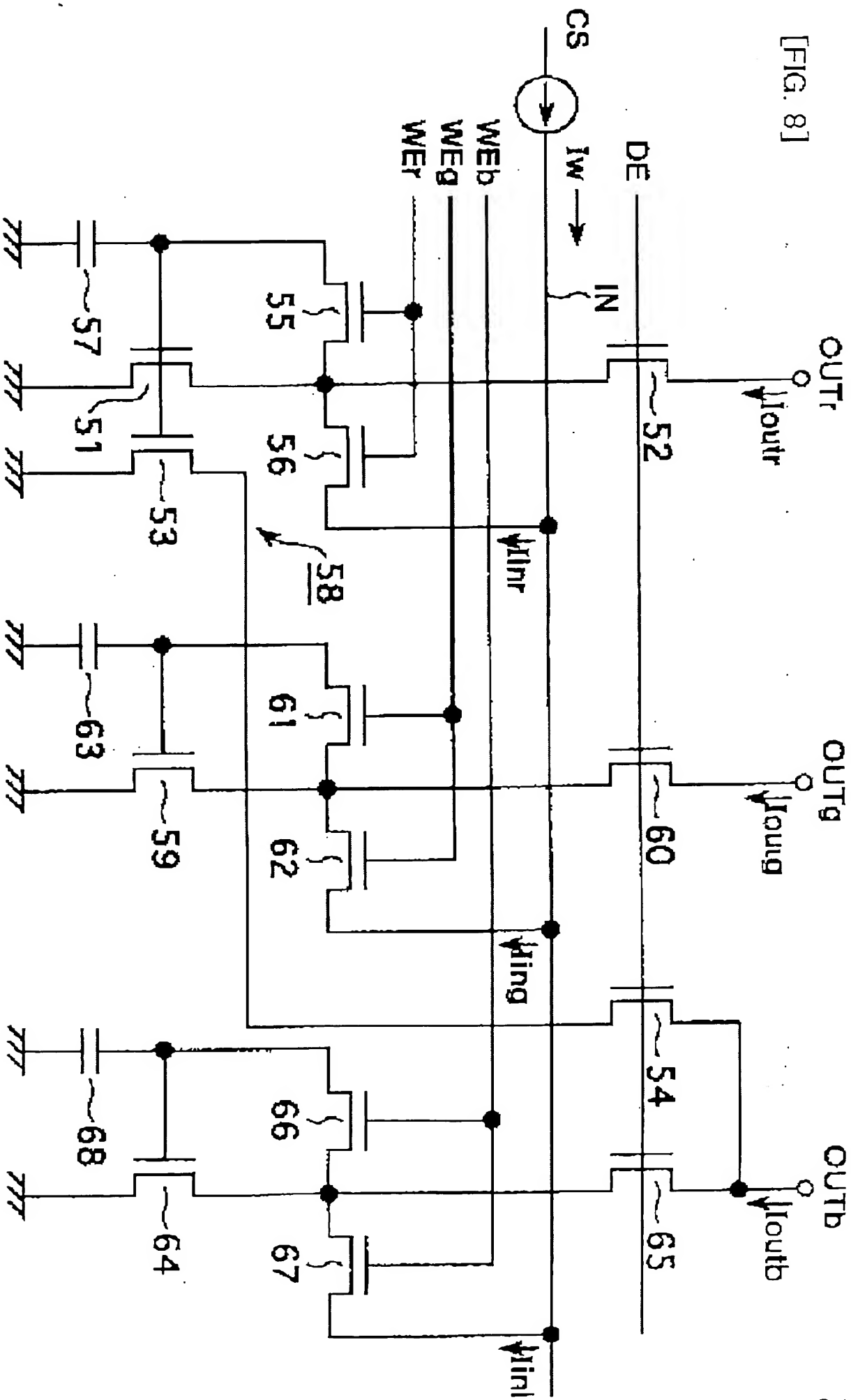
[FIG. 7]


SCAN LINE
Iw
DATA LINE
13
44
45
12
Vcc
46
47
Vcc
CATHODE
GND
42
43
Vcc

[FIG. 8]


CS
Iw
DE
WEr
WEg
WEb
IN
OUTr
Iout r
OUTg
Iout g
OUTb
Iout b
Iin r
Iin g
Iin l
51
52
53
54
55
56
57
58
59
60
61
62
63
64
65
66
67
68

Japanese Unexamined Patent Publication No. 58108/2003 (*Tokukai* 2003-58108)

A. Relevance of the Above-identified Document

The following is a partial English translation of exemplary portions of non-English language information that may be relevant to the issue of patentability of the claims of the present application.

B. Translation of the Relevant Passages of the Document

See also the attached English Abstract.

[EMBODIMENTS]

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[0044]

Used as the pixel circuit 41 is a current write-in type pixel circuit, which is disclosed in International Publication Number WO01/06484 or the like. Fig. 7 illustrates one example of a structure of such a circuit. The current write-in type pixel circuit according to the circuit example uses, e.g., an organic EL element 42 as a display element of the pixel. Luminance of the display element is controlled according to a current. Further, the current write-in type pixel circuit includes (i) four TFTs (insulating gate type thin film field effect transistors) 43 through 46, and (ii) a capacitor 47. The current write-in type pixel circuit receives luminance data from each of the

data lines 13, in the form of a current.

[0045]

Specifically, the organic EL element 42 has a cathode connected to a first power source (e.g., ground). The P-channel TFT 43 has a source connected to a second power source (e.g., a positive power source Vcc), and has a drain connected to the cathode of the organic EL element 42. The N-channel TFT 44 has a drain connected to each of the data lines 13 (13r – 1, 13g – 1, 13b – 1 through 13r – n, and 13b – n), and has a gate connected to each of the scan lines 12 (12 – 1 through 12 – m).

[0046]

The P-channel TFT 45 has a diode connection structure in which a gate and a drain are short-circuited. The gate and the drain of the P-channel TFT 45 are each connected to a source of the TFT 44, and a source of the P-channel TFT 45 is connected to the positive power source Vcc. Further, the N-channel TFT 46 has a drain connected to the gate and the drain of the TFT 45, and has a source connected to a gate of the TFT 43, and has a gate connected to the scan line 12. The capacitor 47 has one end connected to the positive power source Vcc, and has the other end to the gate of the TFT 43.

[0047]

Here, each of the TFTs 44 and 46 serves as an analog switch. The TFT 45 converts (i) a luminance signal current

to be written in, into (ii) a voltage. The capacitor 47 holds the luminance signal voltage, i.e., the voltage which was converted from the current by the TFT 45. The TFT 43 converts (i) the luminance signal voltage held by the capacitor 47 into (ii) a current so as to supply the current to the organic EL element 42. Further, the TFTs 45 and 43 constitute a current mirror circuit.

[0048]

In the current write-in type pixel circuit 41 having such a structure, when the scan line 12 is selected (high level) during the luminance data write-in so as to supply a luminance data current Iw to the data line 13, the luminance data current Iw flows into the TFT 45 via the TFT 44. Because the TFTs 45 and 42 constitute the current mirror circuit, a current proportional to the current flowing into the TFT 45 flows into the TFT 42 on this occasion. Accordingly, the current flows into the organic EL element 42. This causes the organic EL element 42 to emit light.

[0049]

From such a state, the scan line 12 is caused to be unselected (low level). This causes the capacitor 47 to hold a source-drain voltage of the TFT 43. According to the source-drain voltage thus held, the organic EL element 42 is driven, so that the organic EL element 42 keeps on emitting light with the same luminance even after the

scan line 12 becomes unselected.

[0050]

Note that the pixel circuit 41 is not limited to the aforementioned circuit structure, and can be any current write-in type pixel circuit. Moreover, conductivity types of the transistors can be arbitrarily modified.

[0051]

See Fig. 6 again. Outside the pixel portion in which the current write-in type pixel circuits 41 are provided in a matrix manner, there are provided a scan line driving circuit 17 and a data line driving circuit 48, as is the case with a passive matrix color organic EL display apparatus. The scan line driving circuit 17 selectively drives the scan lines 12 – 1 through 12 – m. On the other hand, the data line driving circuit 48 selectively drives the data lines 13r – 1, 13g – 1, 13b – 1 through 13r – n, 13g – n, and 13b – n. The data line driving circuit 48 is made up of the n-number of current write-in type current driving circuits (hereinafter, referred to as simply "current driving circuit") 49 – 1 through 49 – n. Each of the current driving circuits 49 – 1 through 49 – n is provided for every three lines which respectively correspond to R, G, and B.

[0052]

(Second circuit example of the data line driving circuit) Fig. 8 is a circuit diagram illustrating a specific example of the current driving circuits 49 – 1 through 49

– n, which constitute the data line driving circuit 48. The current driving circuit according to the present example uses TFTs as transistors constituting the circuit.

[0053]

The current driving circuit according to the present example includes (i) a signal input line IN, which is common to R, G, and B; and (ii) output terminals OUTr, OUTg, and OUTb of luminance signals that correspond to R, G, and B, respectively. Further, TFTs 51 and 52 are connected in series between a reference potential point (e.g., ground) and the output terminal OUTr. Further, TFTs 53 and 54 are connected in series between the ground and the output terminal OUTb.

[0054]

Further, a TFT 55 is provided between a gate of the TFT 51 and a drain thereof, and a TFT 56 is provided between the drain of the TFT 51 and the signal input line IN. Each of the TFTs 55 and 56 serves as an analog switch when a red write-in control signal Wer is supplied to each gate of the TFTs 55 and 56. Further, a capacitor 57 is provided between the gate of the TFT 51 and the ground. The gates of TFTs 51 and 53 are commonly connected, so that the TFTs 51 and 53 constitute a current mirror circuit 58 when the gate of the TFT 51 and the drain thereof are short-circuited via the TFT 55.

[0055]

Further, TFTs 59 and 60 are provided in series between the ground and the output terminal OUTg. A TFT 61 is provided between a gate of the TFT 59 and a drain thereof. Moreover, a TFT 62 is provided between the drain of the TFT 59 and the signal input line IN. Each of the TFTs 61 and 62 serves as an analog switch when a green write-in control signal Weg is supplied to each gate of the TFTs 61 and 62. Further, a capacitor 63 is provided between the gate of the TFT 59 and the ground.

[0056]

TFTs 64 and 65 are provided in series between the ground and the output terminal OUTg. A TFT 66 is provided between a gate of the TFT 64 and a drain thereof. Moreover, a TFT 67 is provided between the drain of the TFT 64 and the signal input line IN. Each of the TFTs 66 and 67 serves as an analog switch when the green write-in control signal Web is supplied to each gate of the TFTs 66 and 67. Further, a capacitor 68 is provided between the gate of the TFT 66 and the ground.

[0057]

Note that each of the gates of the TFTs 52, 54, 60, and 65 receives a driving control signal DE. The driving control signal DE and the write-in control signals WEr, WEg, and WEb are supplied from a timing control circuit (not shown). Further, the signal input line IN are shared in a time division manner with the driving circuits

corresponding to the colors (R, G, and B), so that luminance signal currents which respectively correspond to the colors are supplied to the signal input line IN in time series.